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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,699	12/05/2003	Young-Hun Seo	OPP 031052 US	9947

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,699	SEO, YOUNG-HUN	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/19/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-15* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05/03&10/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of GroupII (Claims 1-15) on 10/19/2004 is acknowledged.

Claims 16-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10/19/2004.

Drawings

2. Figures 1A-1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2 and 7 are rejected under 35 U. S. C. 102(b) as being anticipated by Liu et al. (US Pat. 6,184,105, herein after Liu).

Regarding claim 1, Liu discloses a method of forming a trench in a semiconductor device, comprising: forming a sacrificial layer on a silicon wafer and selectively etching the sacrificial layer to form a LOCOS opening having a predetermined width; performing thermal oxidation on a portion of the silicon wafer exposed through the LOCOS opening to form a LOCOS oxide layer (conventional LOCOS isolation process, see S.Wolf et al., Silicon Processing for the VLSI Era; Vol. 2-Process Integration, Pages 20-27); etching the LOCOS oxide layer 37 and the silicon wafer to a desired depth to form a trench, the etching being performed such that the LOCOS oxide layer 37 is left remaining on the silicon wafer at an area corresponding to edges of the trench (col. 4, lines 51-57) ; and forming an insulation layer 42 such that the trench is filled with a material of the insulation layer (col. 5, lines 11-19 and figs. 12-13).

Regarding claim 2, Liu discloses during formation of the LOCOS opening, one of a predetermined width of the sacrificial layer located at edges of a region where a trench is to be formed is etched, and the sacrificial layer is etched to a width greater by a predetermined amount than a region to be occupied by a trench (figs. 9-10 and col. 4, lines 51-65).

Regarding claim 7, Liu discloses forming a liner oxide layer 41 prior to forming the insulation layer 42, the liner oxide layer 41 covering inner walls of the trench and the remaining region of the LOCOS oxide layer (figs. 9-10 and col. 5, lines 4-11).

4. Claims 1, 5,11, 13 and 14 are rejected under 35 U. S. C. 102(e) as being anticipated by Park (US Pat. 6,566,207).

Regarding claim 1, Park discloses in col. 6, lines 26-66 a method of forming a trench in a semiconductor device, comprising: forming a sacrificial layer 204 on a silicon wafer and selectively etching the sacrificial layer to form a LOCOS opening having a predetermined width (fig. 5A); performing thermal oxidation on a portion of the silicon wafer exposed through the LOCOS opening to form a LOCOS oxide layer (fig. 5B); etching the LOCOS oxide layer and the silicon wafer to a desired depth to form a trench, the etching being performed such that the LOCOS oxide layer is left remaining on the silicon wafer at an area corresponding to edges of the trench (fig. 5C); and forming an insulation layer such that the trench is filled with a material of the insulation layer 212 (fig. 5D).

Regarding claim 5, Park discloses during formation of the trench, a photoresist layer is deposited on the LOCOS oxide layer and the sacrificial layer, then the photoresist layer is exposed and developed to form a photoresist layer pattern that exposes an area of the LOCOS oxide layer where a trench is to be formed, after which the photoresist layer pattern is used as a mask to etch the exposed area of the LOCOS oxide layer and the silicon wafer to a desired depth (figs. 5A-5C).

Regarding claim 11, Park discloses performing chemical-mechanical polishing on the insulation layer following the formation of the same until the sacrificial layer is exposed (col. 6, lines 62-66).

Regarding claims 13 and 14, Park discloses the sacrificial layer 204 is made of a material (nitride) that is polished more slowly than the insulation layer that fills the trench 212 (oxide) (col. 6, lines 62-66).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 4 and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Liu et al. (US Pat. 6,184,105, herein after Liu).

Liu discloses a method of forming a trench in a semiconductor device but fails to disclose the sacrificial layer is etched to a width of 50-500Å (claim 3); the sacrificial layer is etched having a width that is at most 400Å greater than the trench (claim 4); and the liner oxide layer is formed to a thickness of 100-500 Å (claim 8). Although the exact width of the trench and the thickness of the liner oxide was not specified as recited in claims 3, 4 and 8, it appears that having a specific width and thickness as claimed is prima facie obvious due to the fact that one

can vary the width and thickness in order to achieve a specific trench dimension in a semiconductor device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Liu by selecting a suitable width and thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, as the width of the trench and the thickness of the oxide liner does seem to be critical to the invention, it must be shown that any one or all of the listed materials yield an unexpected product or result. In re Margolis 228 USPQ 940 (Fed. Cir. 1986); In re Kirsch 182 USPQ 286 (CCPA 1974); In re Suether 181 USPQ 36 (CCPA 1974); In re Costello 178 USPQ 290 (CCPA 1973); In re Von Schickh 150 USPQ 300 (CCPA 1966); In re Sussman 60 USPQ 538 (CCPA 1944); In re Kaplan 45 USPQ 175 (CCPA 1940).

6. Claims 6 and 15 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Park et al. (US Park (6,566,207).

Park discloses a method of forming a trench in a semiconductor device but fails to disclose at most 200Å of a width of the LOCOS oxide layer positioned at edges of the trench is covered such that at most 400Å of an entire cross-sectional width is covered (claim 6); and the thickness of the SiN sacrificial layer (claim 15). Although the exact thickness of the sacrificial layer and the cross-sectional width of the trench was not specified as recited in claim 15 and claim 6, it appears that having a specific width and thickness as claimed is prima facie obvious

due to the fact that one can vary the width and thickness in order to achieve a specific trench dimension in a semiconductor device.

Allowable Subject Matter

7. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

December 16, 2004.